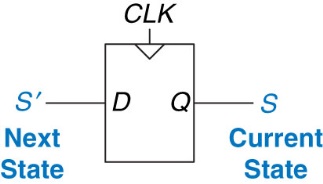
**Lesson 15 – Finite State Machines (FSM) - Design**

From Last Time:

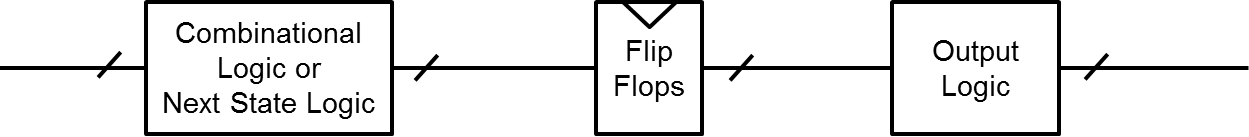
* What do Flip-Flops Create?
* When do they do this?

**Finite State Machine (FSM) Makeup: M – \_\_\_\_\_\_\_\_\_\_ , N – \_\_\_\_\_\_\_\_\_\_, and K -\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

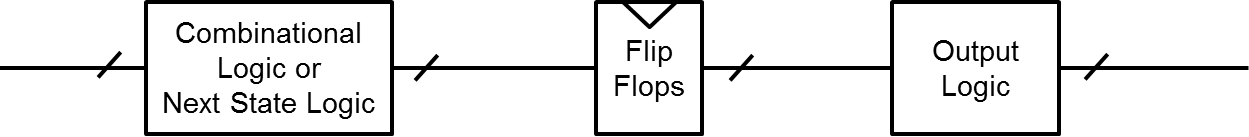


**Two Types of FSMs:**

**\_\_\_\_\_\_\_\_\_\_\_\_ Machine** –



**\_\_\_\_\_\_\_\_\_\_\_\_ Machine** –



**How to Design a State Machine:**

Real Life Examples of State Machines:







**FSM Example – Vending Machine:**

**Step 0) Description**

* **Only takes Quarters. Only sells (insert favorite drink).**
* **No change. 50₵ per Soda**
* **Inputs: C = Coin (also, there’s a clock)**
* **Outputs: S = Soda**

**Step 1)**

**Step 2)**

**Step 3)**

**Step 4)**

**FSM Example – Vending Machine:**

**Step 0) Description**

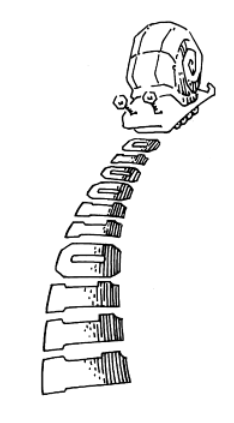
* **Only takes Quarters.**
* **No change. 50₵ per Soda**
* **Inputs: C = Coin (also, there’s a clock)**
* **Outputs: S = Soda**

**Step 1)**

**Step 2)**

**Step 3)**

**Step 4)**

**Boardwork:**

* Draw me a picture of a Mealy or Moore State Transition Diagram that shows
* A Snail is crawling across a sequence of numbers and he smiles if the last 2 numbers are “11”
* Sequence: 0100110111

Synchronous circuit – Combinational circuit followed by bank of flip flops

Properties: a) Each element is either a register or a combinational circuit

b) At least one circuit is a register

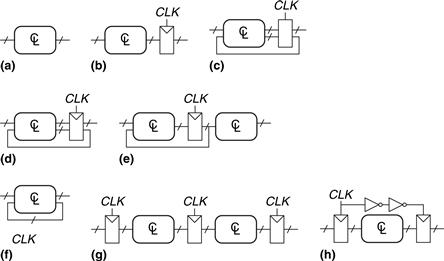
c) All registers have the same clock

d) Every cyclic path contains at least one register

Example: FSMs, Pipelines

Asynchronous circuit – Timing not limited by clock registers

**Example 3.5: Synchronous Sequential Circuits**



**Solutions**

**Circuit:**

* (a) is combinational, not sequential, because it has no registers.
* (b) is a simple sequential circuit with no feedback.
* (c) is neither a combinational circuit nor a synchronous sequential circuit, because it has a latch that is neither a register nor a combinational circuit.
* (d) and (e) are synchronous sequential logic; they are two forms of finite state machines, which are discussed in Section 3.4.
* Same as (d)
* (f) is neither combinational nor synchronous sequential, because it has a cyclic path from the output of the combinational logic back to the input of the same logic but no register in the path.
* (g) is synchronous sequential logic in the form of a pipeline, which we will study in Section 3.6.
* (h) is not, strictly speaking, a synchronous sequential circuit, because the second register receives a different clock signal than the first, delayed by two inverter delays.